

REMARKS

Claims 1-7, 10-16 and 19-23 are pending in the application.

Claims 1-7, 10-16 and 19-23 have been rejected.

Claims 1, 10 and 19 have been amended as set forth herein.

Claims 1-7, 10-16 and 19-23 remain pending in this application.

Reconsideration of the claims is respectfully requested.

I. CLAIM REJECTIONS -- 35 U.S.C. § 103

Claims 1, 6, 7, 10, 15, 16 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Publication No. 2003/0231625 to *Calvignac, et al.*, (hereinafter “Calvignac”) in view of U.S. Patent No. 7,415,540 to *Fallon et al.*, (hereinafter “Fallon”). Claims 2, 5, 11, 14, 20 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Calvignac reference in view of Fallon, and further in view of U.S. Patent No. 7,197,035 to *Asano*, (hereinafter “Asano”). Claims 3, 4, 12, 13, 21 and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Calvignac reference in view of Fallon, and further in view of U.S. Patent Publication No. 2004/0100956 to *Watanabe*, (hereinafter “Watanabe”). The Applicants respectfully traverse the rejections.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142, p. 2100-133 (8th ed. rev. 4, October 2005). Absent such a *prima facie* case, the applicants are under no obligation to produce evidence of nonobviousness. *Id.* To establish a *prima facie* case of obviousness, three basic criteria must be

met: *Id.* First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. *Id.* Second, there must be a reasonable expectation of success. *Id.* Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *Id.* The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicants' disclosure. *Id.*

Amended independent Claim 1 recites a router that includes a switch fabric and a plurality of routing nodes. Each routing node includes first and second network processors that include respective first and second pluralities of microengines. Each of the first and second pluralities of microengines are for performing respective first and second security and classification functions associated with data packets, where each data packet is distributed to a selected microengine. The first network processor receives data packets from external devices and transmits data packets to the switch fabric. The second network processor receives data packets from the switch fabric and transmits data packets to the external devices. Each routing node also has a routing table search circuit that includes an initial content addressable memory stage followed by a plurality of trie tree search table stages. The Applicants respectfully submit that the cited references do not describe such a router.

The Examiner asserted that Calvignac describes a router that includes a switch fabric and a plurality of routing nodes, where each routing node includes first and second network processors. Calvignac is further asserted to describe each of the first and second network processors as

performing respective first and second security and classification functions associated with data packets, where the first network processor receives data packets from external devices and transmits data packets to the switch fabric and the second network processor receives data packets from the switch fabric and transmits data packets to the external devices.

The Examiner acknowledged that Calvignac does not disclose the first and second network processors including respective first and second pluralities of microengines that, respectively, perform the first and second security and classification functions, where each data packet is distributed to a selected microengine. The Examiner asserted that Fallon describes a router implemented using a microprocessor that includes multiple microengines, where packets are assigned to a selected microengine. However, the Applicants respectfully submit that none of the cited references describe a router that includes routing nodes having a routing table search circuit that includes an initial content addressable memory stage followed by a plurality of trie tree search table stages, as recited in amended independent Claim 1.

For at least these reasons, the prior art references cited by the Examiner do not teach or suggest the unique and novel limitations recited in independent Claim 1, as amended. Amended independent Claims 10 and 19 recite limitations that are analogous to the unique and novel limitations cited in Claim 1 and are also patentable over the cited prior art references. Additionally, dependent Claims 2-7, 11-16, and 20-23 depend from the independent Claims 1, 10 and 19, respectively, and contain all of the unique and novel limitations recited in Claims 1, 10 and 19, respectively. This being the case, these dependent claims are also patentable over the cited prior art references.

Accordingly, the Applicants respectfully request that the Examiner withdraw the § 103 rejection with respect to these claims.

CONCLUSION

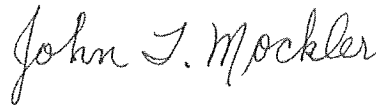
As a result of the foregoing, the Applicants assert that the remaining claims in the Application are in condition for allowance, and respectfully requests an early allowance of such claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *jmockler@munckcarter.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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